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IN THE CLAIMS:

20. (Amended) A method of manufacturing a semiconductor storage device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a conductive film on said first insulating film;

forming a protective film on said conductive film;

etching said protective film and said conductive film locally and forming first and second wirings;

forming a second insulating film between said first and second wirings;

etching said second insulating film and said first insulating film locally by using said protective film as a mask and forming a contact hole between said first and second wirings; and

forming a third insulating film at least on a side wall of said conductive film and on a side wall of said first insulating film in said contact hole, wherein said third insulating film is in physical contact with the side walls of said conductive film and said first insulating film in said contact hole.

21. (Amended) ~~A~~ The method according to claim 20, wherein said step of forming said second insulating film between said first and second wirings comprises the steps of:

depositing said second insulating film on a whole surface; and

etching said second insulating film up to ~~an~~ the upper surface of said protective film and removing it and planarizing the surface.

22. (Amended) ~~A~~ The method according to claim 20, wherein said step of etching said second insulating film and said first insulating films locally using said protective film as a mask and forming said contact hole between said first and second wirings comprises the steps of:

forming a linear/space photo-resist which intersects perpendicularly to said first and second wirings; and

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etching said second and first insulating films locally using said photo-resist and said protective film as a mask.

23. (Amended) A-The method according to claim 20, wherein said protective film is composed of a silicon nitride film, and the silicon nitride film is removed after said third insulating film is formed.

24. (Amended) A-The method according to claim 20, wherein said protective film is composed of one of a second conductive film and a metallic film, and one of the second conductive film and the metallic film is removed after said third insulating film is formed.

25. (Amended) A-The method according to claim 20, wherein said protective film is composed of a second conductive film, said method further comprising:

~~wherein said step of forming said protective film comprises the step of forming a third conductive film on said second conductive film, said second insulating film and in said contact hole after said third insulating film is formed;~~ and ~~the step of~~

etch-backing said third conductive film and said second conductive films and removing said second conductive film and filling up said contact hole with said third conductive film.

26. (Amended) A-The method according to claim 20, wherein said protective film is composed of a second conductive film, said method further comprising:

~~wherein said step of forming said protective film comprises the step of forming a third conductive film on said second conductive film, and said second insulating film and in said contact hole after said third insulating film is formed;~~ and ~~the step of~~

etching and removing a portion of said third conductive film and said second conductive films when said third conductive film is patterned by using a predetermined storage node electrode pattern.

27. (Amended) A method of manufacturing a semiconductor storage device comprising the steps of:

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forming an element separation insulating film on a semiconductor substrate, for dividing an element region;

forming a gate electrode on the element region divided by said element separation insulating film, connected to a gate insulating film and a word line, and an MOS transistor having a source/drain regions;

forming a first insulating film for covering said MOS transistor and said element separation insulating film;

etching said first insulating film locally and forming a first contact hole reaching a first ~~one of the~~ source/drain regions of said MOS transistor and a second contact hole reaching a second ~~the other~~ source/drain region of said MOS transistor, said first contact hole being formed on the element region and on said element separation insulating film, and said second contact hole being formed on the element region, said first and second contact holes being self-aligned with said gate electrode;

forming first and second conductive plugs for filling up said first and second contact holes;

forming a second insulating film for covering said first insulating film and said first and second conductive plugs;

etching said second insulating film locally and forming a bit line contact reaching said first conductive plug on said element separation insulating film;

forming a bit line, ~~whose~~ having a lower section ~~is composed of~~ a conductive film and an upper section ~~is composed of~~ a third insulating film, on said second insulating film and said bit line contact;

forming a fourth insulating film on said second insulating film and said bit line;

etching said fourth insulating film and said second insulating film locally by using said third insulating film as a mask and forming a storage node contact reaching said second conductive plug so that said storage node contact is self-aligned with said bit line;

forming a fifth insulating film on a side wall of the conductive film of said bit line and a side wall of said second insulating film in said storage node contact; and

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forming a storage node electrode, a capacitor insulating film on said storage node electrode and a plate electrode on said capacitor insulating film in this order so as to form a capacitor, said storage node electrode connected to said second conductive plug and electrically separated from the conductive film of said bit line by said fifth insulating film.

28. (Amended) A-The method according to claim 27, wherein said step of forming said fourth insulating film on said second insulating film and said bit line comprises the step of:

depositing said fourth insulating film on the whole surface; and
etching and removing said fourth insulating film up to an upper surface of said third insulating film so as to level the surface.

29. (Amended) A-The method according to claim 27, wherein said step of etching said fourth insulating film and said second insulating film locally by using said third insulating film as a mask and forming a storage node contact reaching said second conductive plug so that said storage node contact is self-aligned with said bit line, comprises the steps of:

forming a linear/space photo-resist which intersects perpendicularly to said bit line; and
etching said fourth insulating film and said second insulating film locally by using said photo-resist and said third insulating film as a mask.

34. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming an element separation insulating film in a semiconductor substrate for dividing an element region;

forming a transistor in said element region, said transistor having a gate insulating film, a gate electrode connected to a word line and a source/drain region;

forming a first insulating film, said first insulating film covering said element separation insulating film and said transistor;

forming a first contact hole in said first insulating film, said first contact hole reaching a first region of said source/drain region of said transistor;

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forming a second contact hole in said first insulating film, said second contact hole reaching a second region of said source/drain region of said transistor;

forming a first conductive plug for filling up said ~~first~~first contact hole;

forming a second conductive plug for filling up said second contact hole;

forming a second insulating film, said second insulating film covering said first insulating film and said first and second conductive plugs;

forming a bit line contact in said second insulating film, said bit line contact reaching said first conductive plug;

forming a bit line in said second insulating film and said bit line contact, a lower part of said bit line including a conductive film and an upper part including a third insulating film;

forming a fourth insulating film on said second insulating film and said bit line;

forming a contact hole for a storage node on a side of said bit line and through said fourth insulating film and said second insulating film, said contact hole reaching said second conductive plug;

forming a fifth insulating film at least on a side wall of said conductive film and a side wall of said second insulating film on said bit line exposed from said contact hole; and

forming a capacitor having a storage node, a plate electrode above said storage node and a capacitor insulating film formed therebetween, said storage node being electrically separated from said conductive film by said fifth insulating film and connected to said second conductive plug via said contact hole,

wherein said contact hole for said storage node is defined by a line/space pattern which intersects perpendicularly to said bit line.

